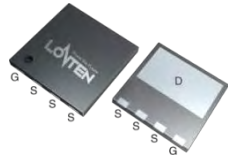
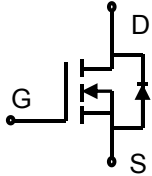



## LonTen N-channel 650V, 20A, 0.18Ω LonFET™ Power MOSFET

<p><b>Description</b> LonFET™ Power MOSFET is fabricated using advanced super junction technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.</p> <p><b>Features</b></p> <ul style="list-style-type: none"> <li>◆ Ultra low <math>R_{DS(on)}</math></li> <li>◆ Ultra low gate charge (typ. <math>Q_g = 39\text{nC}</math>)</li> <li>◆ 100% UIS tested</li> <li>◆ RoHS compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>◆ Power factor correction (PFC).</li> <li>◆ Switched mode power supplies (SMPS).</li> <li>◆ Uninterruptible power supply (UPS).</li> </ul>	<p><b>Product Summary</b></p> <table> <tr> <td><math>V_{DS} @ T_{j,max}</math></td> <td>700V</td> </tr> <tr> <td><math>R_{DS(on),max}</math></td> <td>0.18Ω</td> </tr> <tr> <td><math>I_{DM}</math></td> <td>60A</td> </tr> <tr> <td><math>Q_{g,typ}</math></td> <td>39nC</td> </tr> </table> <p><b>Pin Configuration</b></p>  <p><b>DFN8x8</b></p>  <p>N-Channel MOSFET </p>	$V_{DS} @ T_{j,max}$	700V	$R_{DS(on),max}$	0.18Ω	$I_{DM}$	60A	$Q_{g,typ}$	39nC
$V_{DS} @ T_{j,max}$	700V								
$R_{DS(on),max}$	0.18Ω								
$I_{DM}$	60A								
$Q_{g,typ}$	39nC								

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	650	V
Continuous drain current ( $T_C = 25^\circ\text{C}$ )	$I_D$	20	A
( $T_C = 100^\circ\text{C}$ )		13	A
Pulsed drain current <sup>1)</sup>	$I_{DM}$	60	A
Gate-Source voltage	$V_{GSS}$	$\pm 30$	V
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	600	mJ
Power Dissipation	$P_D$	108	W
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Continuous diode forward current	$I_S$	20	A
Diode pulse current	$I_{S,pulse}$	60	A

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.15	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient <sup>3)</sup>	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Soldering temperature, wavesoldering only allowed at leads. (1.6mm from case for 10s)	$T_{sold}$	260	$^\circ\text{C}$

## Package Marking and Ordering Information

Device	Device Package	Marking	Units/Reel
LSNC65R180GT	DFN 8×8	LSNC65R180GT	3000

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static characteristics</b>						
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0 V, I <sub>D</sub> =0.25 mA	650	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =0.25mA	2.5	3.5	4.5	V
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =650 V, V <sub>GS</sub> =0 V, T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C	- -	- 10	1 -	μA
Gate leakage current, Forward	I <sub>GSSF</sub>	V <sub>GS</sub> =30 V, V <sub>DS</sub> =0 V	-	-	100	nA
Gate leakage current, Reverse	I <sub>GSSR</sub>	V <sub>GS</sub> =-30 V, V <sub>DS</sub> =0 V	-	-	-100	nA
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10 V, I <sub>D</sub> =10 A T <sub>J</sub> = 25°C T <sub>J</sub> = 150°C	- - -	0.16 0.4	0.18 -	Ω
Gate resistance	R <sub>G</sub>	f=1 MHz, open drain	-	4.4	-	Ω
<b>Dynamic characteristics</b>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2637	-	pF
Output capacitance	C <sub>oss</sub>		-	1250	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	17	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 380V, I <sub>D</sub> = 10A R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> =10V	-	23	-	ns
Rise time	t <sub>r</sub>		-	33	-	
Turn-off delay time	t <sub>d(off)</sub>		-	113	-	
Fall time	t <sub>f</sub>		-	11	-	
<b>Gate charge characteristics</b>						
Gate to source charge	Q <sub>gs</sub>	V <sub>DD</sub> =480 V, I <sub>D</sub> =10A, V <sub>GS</sub> =0 to 10 V	-	10.3	-	nC
Gate to drain charge	Q <sub>gd</sub>		-	13.7	-	
Gate charge total	Q <sub>g</sub>		-	39	-	
Gate plateau voltage	V <sub>plateau</sub>		-	5.5	-	V
<b>Reverse diode characteristics</b>						
Diode forward voltage	V <sub>SD</sub>	V <sub>GS</sub> =0 V, I <sub>F</sub> =10A	-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	V <sub>R</sub> =50 V, I <sub>F</sub> =20A, dI <sub>F</sub> /dt=100 A/μs	-	345	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	3.8	-	μC
Peak reverse recovery current	I <sub>rrm</sub>		-	22	-	A

### Notes:

- Limited by maximum junction temperature, maximum duty cycle is 0.75.
- I<sub>AS</sub> = 5A, L=48mH, V<sub>DD</sub> =60V, Starting T<sub>J</sub> = 25°C.
- Weld the device to a PCB board with the size of 32mm\*36mm and then place it in an one-cubic-foot air static box.

### Electrical Characteristics Diagrams

Figure 1. On-Region Characteristics

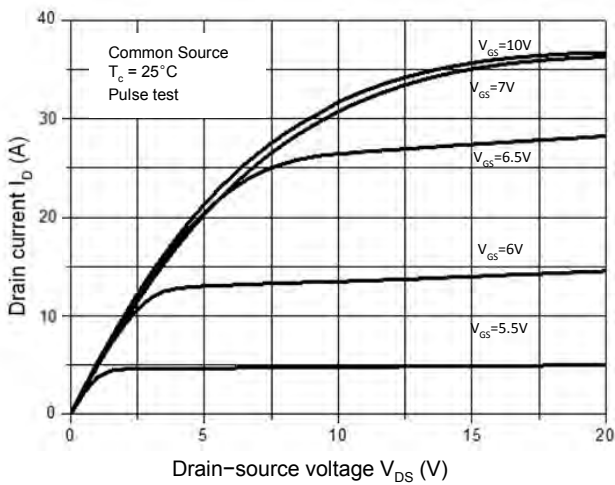


Figure 2. Transfer Characteristics

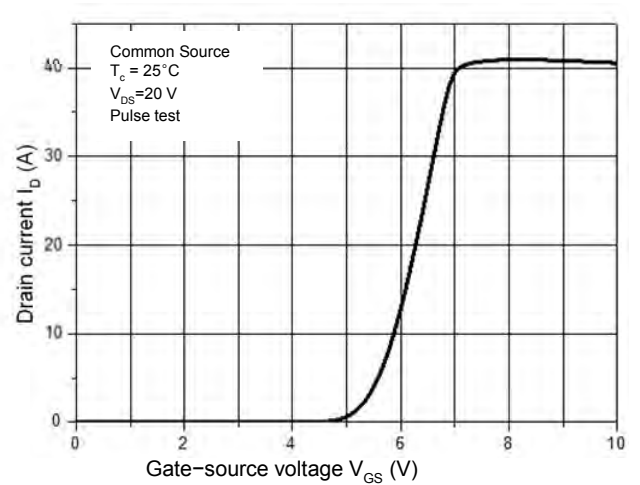


Figure 3. On-Resistance Variation vs. Drain Current

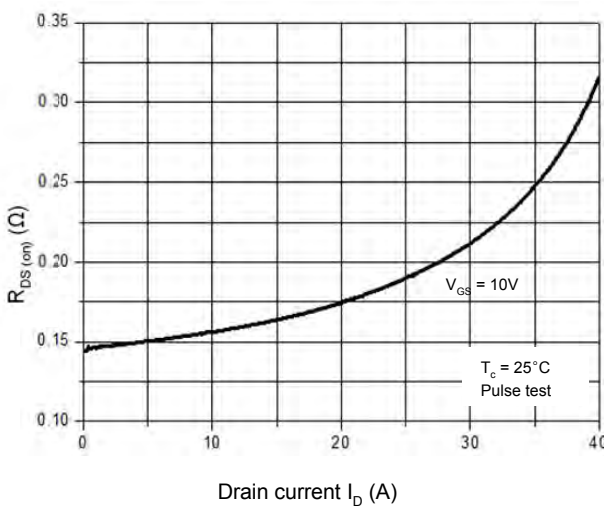


Figure 4. Threshold Voltage vs. Temperature

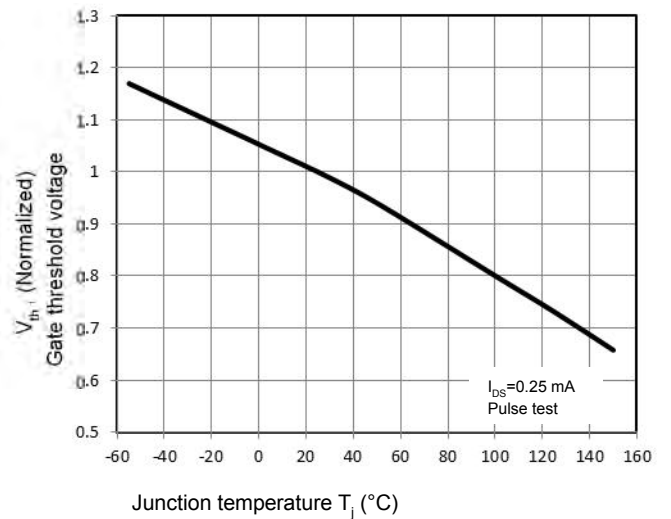


Figure 5. Breakdown Voltage vs. Temperature

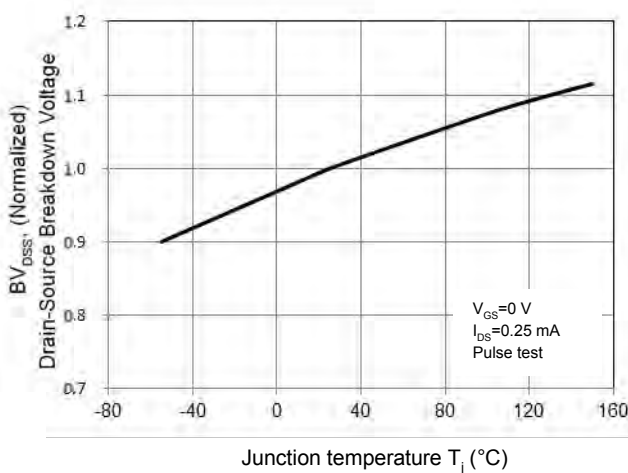


Figure 6. On-Resistance vs. Temperature

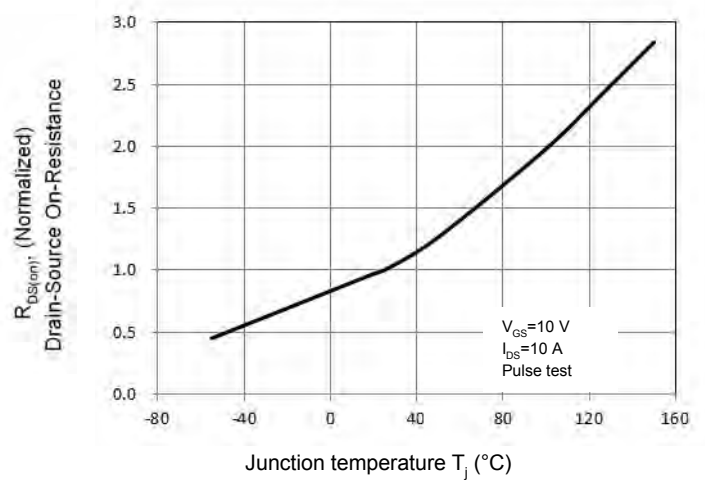


Figure 7. Capacitance Characteristics

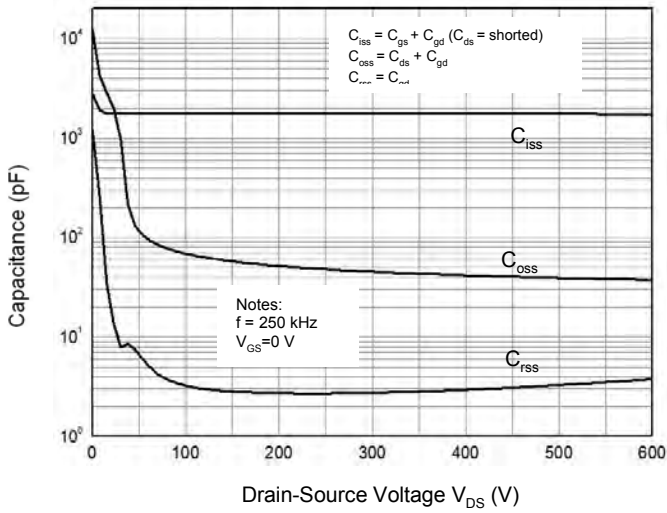


Figure 8. Gate Charge Characteristics

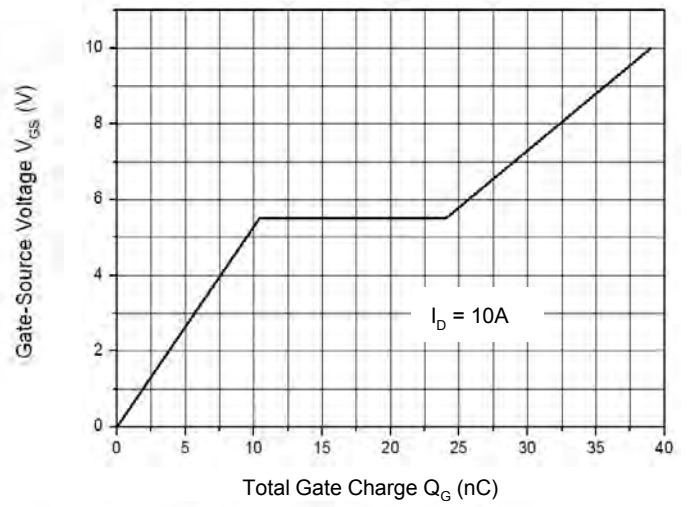


Figure 9. Power Dissipation vs. Temperature

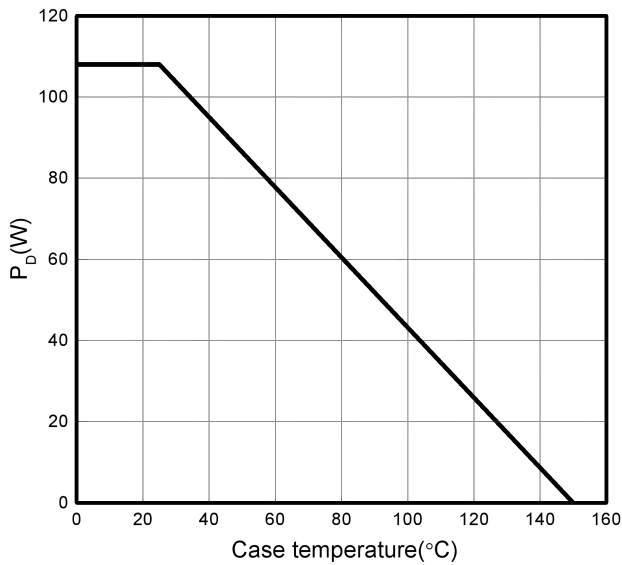


Figure 10: Safe Operating Area

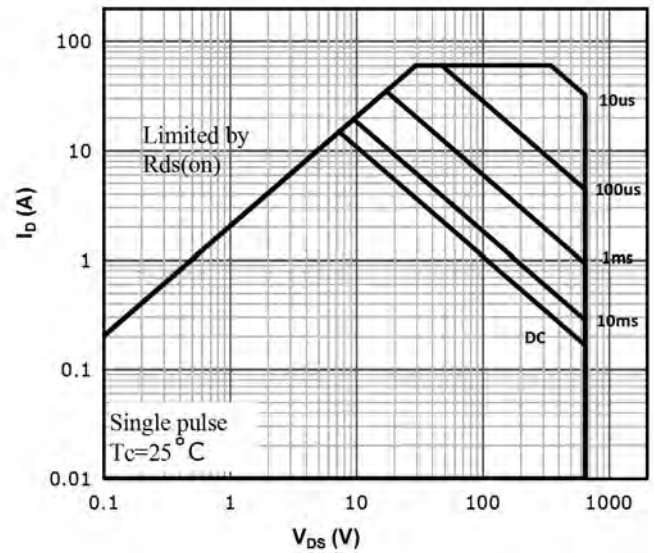
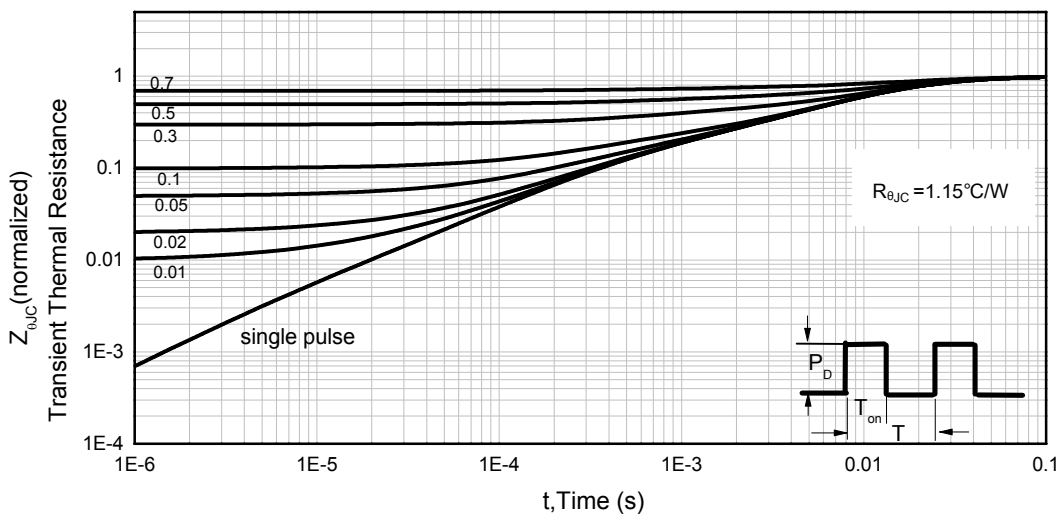
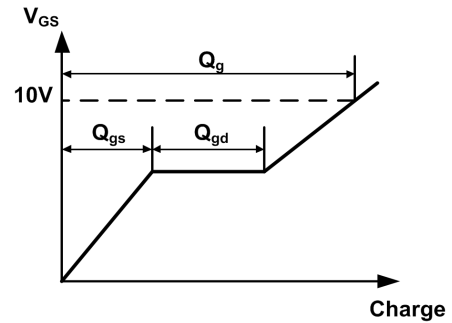
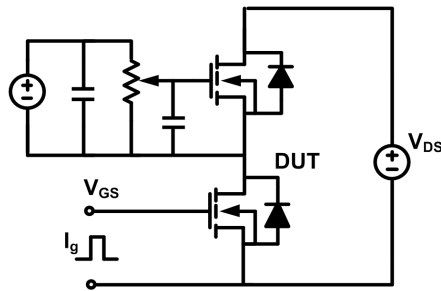


Figure 11. Normalized Maximum Transient Thermal Impedance (RthJC)

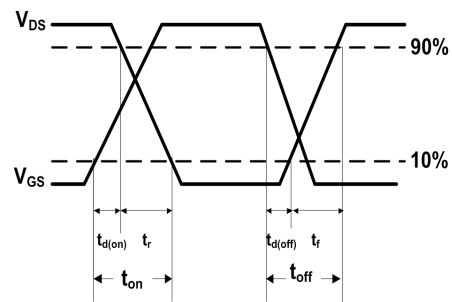
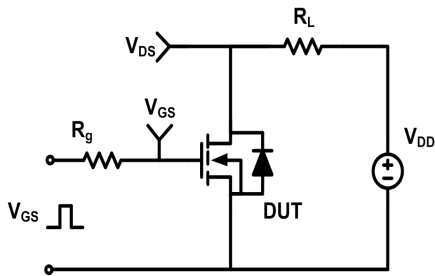


Test Circuit & Waveforms

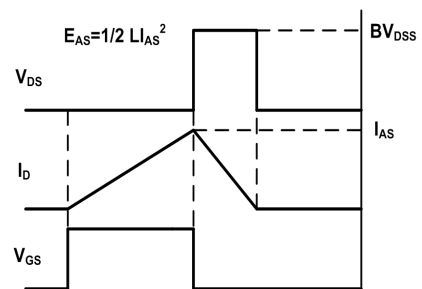
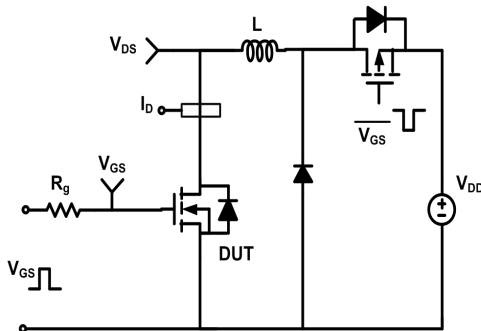
Gate Charge Test Circuit & Waveform



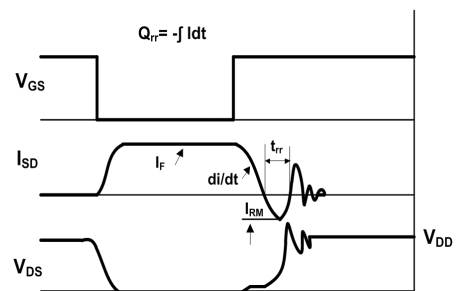
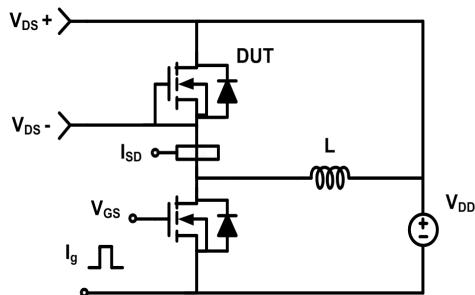
Resistive Switching Test Circuit & Waveform



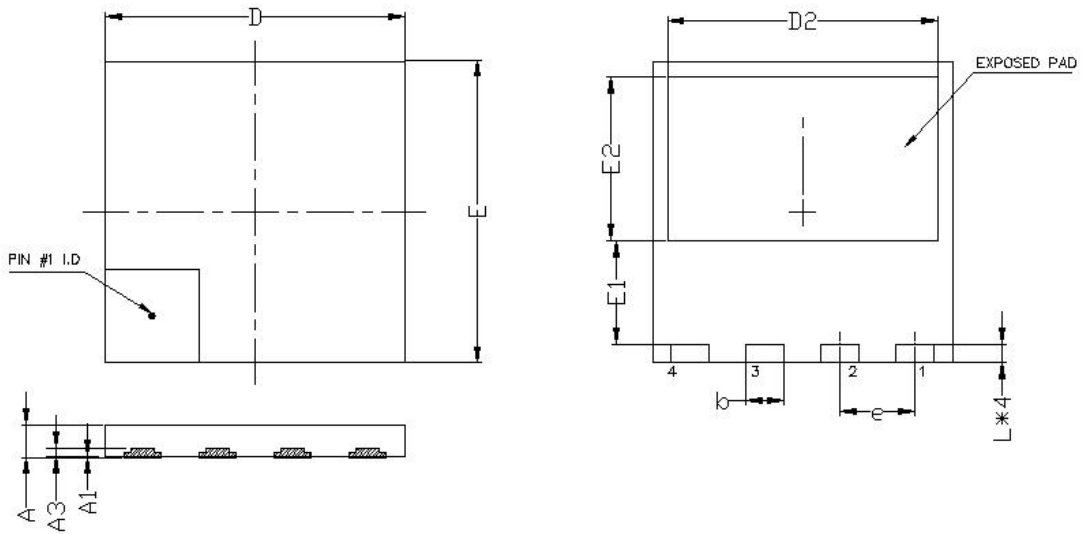
Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Diode Recovery Test Circuit & Waveform



Mechanical Dimensions for DFN8×8



DIMENSIONS IN MILLIMETERS		
SYMBOL	MIN	MAX
A	0.75	1.00
A1	0.00	0.05
A3	0.10	0.30
b	0.90	1.10
D	7.90	8.10
E	7.90	8.10
D2	7.10	7.30
E1	2.65	2.85
E2	4.25	4.65
e	2.00BSC	
L	0.4	0.6